Amendments to the Specification:

Please amend the specification as follows:

Please replace paragraph starting at page 3, line 1, with the following rewritten paragraph:

If a process from deposition to etching of a film serving as offset spacers is performed only once, their thicknesses are the same. However, if the process is done two times, effective offset spacers of different thicknesses can be formed. More specifically, first, a first offset spacers are formed on either side of each of the gate electrodes of the nMOSFET and pMOSFET. Then, an extension region is formed in one of the MOSFETs. Next second offset spacers are formed on the first offset spacers. After that, another extension region is formed in the other MOSFET. Through the above process, the effective offset spacers can be varied in thickness between the nMOSFET and pMOSFET (see, for example, K. Ohta and H. Nakaoka, ~~"Low Gate Leak and High Performance in 80 nm CMOSFET using Double Offset Sidwall,"~~ "Double Offset Implantation Technique for High Performance 80nm CMOSFET With Low Gate Leakage Current", SEMI Forum Japan 2002, ULSI Technology Seminar, Section 4, pp. 42-47).